Indian Institute of Technology Bhubaneswar

School of Electrical and Computer Sciences | ECE Department

SHORT TERM COURSE · 5 DAYS

Advanced Circuit Design Techniques for Analog and Mixed Signal IC Design

Hands-on Training on Cadence EDA Tools

Dates: 15 – 19 December 2026 | **Venue:** IIT Bhubaneswar | **Mode:** In person

30 h Contact hours | **15 h** Hands-on Cadence labs | **30** Seats only

About the Course

Analog circuit design in deep-submicron technologies needs design methods that go beyond square-law hand analysis. This 5-day course combines **3 hours of lectures** with **3 hours of hands-on lab sessions** every day on Cadence Virtuoso, ADE and Spectre. Participants carry one design from device characterisation to a post-layout verified block.

Course Content Highlights

- g_m/I_D-based design methodology for nanoscale CMOS
- Mismatch and non-idealities in analog circuits
- High-gain OTAs and multi-stage compensation
- Fully differential circuits and common-mode feedback
- Switched-capacitor circuits
- Bandgap references and LDO regulators
- Analog layout for matching and parasitic extraction
- PVT corners and Monte Carlo verification on Cadence

Course Instructors



Prof. Bibhu Datta Sahoo

Professor, University at Buffalo, USA

He joined the University at Buffalo as Professor in Fall 2023. He received his B.Tech from IIT Kharagpur (1998), MSEE from the University of Minnesota (2000) and PhD from UCLA (2009). He designed signal-processing ICs at Broadcom (2000–2006) and RF ICs for CMOS TV tuners at MaxLinear (2008–2010), and was a faculty member at IIT Kharagpur for 6 years and Amrita University for 5 years. His research covers mixed-signal circuit design, analog computing and machine learning hardware. He received the 2008 Analog Devices Outstanding Student Designer Award and the 2013 CICC Best Paper Award. He has served as Associate Editor of IEEE TCAS-II and IEEE OJCAS, and is an IEEE CASS Distinguished Lecturer (2025–2026).



Dr. Nijwm Wary

Assistant Professor, IIT Bhubaneswar

B.Tech, M.Tech and PhD from IIT Kharagpur, followed by postdoctoral research on high-speed serial links at the University of Toronto (2018–2019). At IIT Bhubaneswar since 2020, he works on high-speed serial links, on-chip DC-DC converters, PLLs and ADCs. He received the institute's Teaching Excellence Award in 2022.



Dr. Saroj Rout

Professor, Silicon University, Odisha

BE and ME from BITS Pilani and PhD from Tufts University, USA. Over 22 years of experience in CMOS analog circuit design. As an analog IC design engineer at Silicon Laboratories, Austin, USA (2000–2007), he designed circuits for products including DAA and SLIC chips that have sold over 2 billion units. He founded Mixignal Innovations, USA (2009), and co-founded the NSF-funded startup Boston Microtechnology (2014).

Who Can Attend

- BTech (preferably final year), MTech and PhD students
- Faculty members of engineering institutes
- Engineers from industry and R&D labs

Prerequisite: basics of MOSFETs, amplifiers and feedback. No prior Cadence experience is needed.

Registration Fee

Students (UG / PG / PhD)	**Rs. 5,000**
Faculty / Industry professionals	**Rs. 10,000**

Fees include GST. Accommodation and food are not included.

How to Register

- Pay the fees directly to CEP IIT Bhubaneswar with the link below
  https://payments.billdesk.com/bdcollect/bd/iitbhubaneswarresearchinternshipforfaculty/17195
- Register online: **Click here to register**
- Last date of registration: 5th Dec, 2026. Selection is on a first-come, first-served basis

Course Coordinator

Dr. Nijwm Wary, Assistant Professor, ECE Department, IIT Bhubaneswar (nijwmwary@iitbbs.ac.in)

Scan to Register

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